	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	523	dram same (pipelin$)	USPAT	1999/11/21 22:39
2	BRS	L3	154	1 same mode	USPAT	1999/11/21 22:54
3	BRS	L5	24	1 [ab,ti]	USPAT	1999/11/21 23:21
4	BRS	L7	59	1 and (pipeline$ near3 mode)	USPAT	1999/11/21 23:43
5	BRS	L9	19	1 and (pipeline$ near3 page)	USPAT	1999/11/21 23:44

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DATE FILED: **Oct. 3, 1994**

DETDESC:

DETD(61)

FIGS. . . . display processing module 13 feeds the sequencer 143 the control information 1421 for such 16-word read. As a result, the **mode** register 30 has its **burst** length set to 8 (i.e., Mo at T11). The read command is issued at every 8 words (i.e., Re-a at. . . at T22) are issued to the synchronous DRAM 22 so that their processings are executed at the side of the **memory** bank B(b). As a result, the data can be processed in the **pipeline** manner to improve the bus throughput. In other words, the data can be read out without any interruption even at the change of the **memory** banks to be accessed. The display processing module 13 instructs the setting of the **mode** register 30, when it reads out the necessary display data, and executes the precharge S3 (i.e., Pr-ab at T32), the **mode** register setting S7 (i.e., Mo at T33) and the NOP S2 (i.e., Nop at T34) to set the **burst** length to 1. The display processing module 13 then negates the bus demand signal to open the buses.